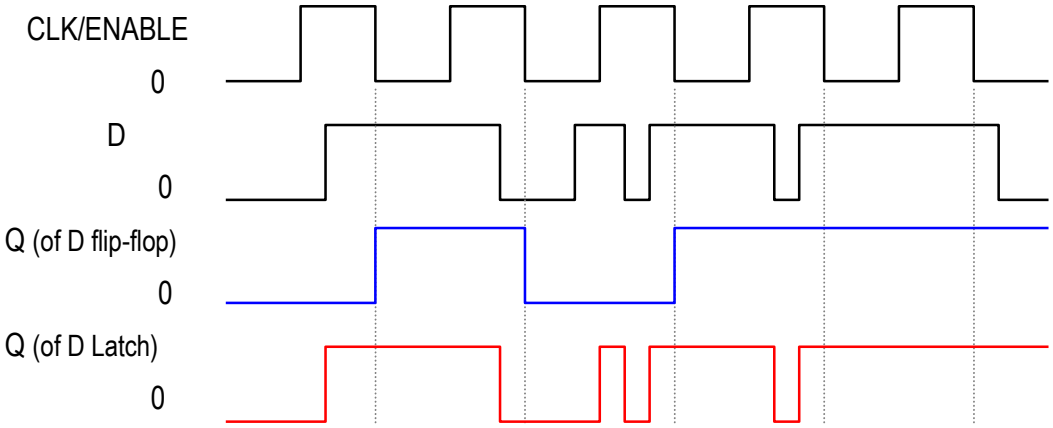
Tutorial 6 (SOLUTIONS)

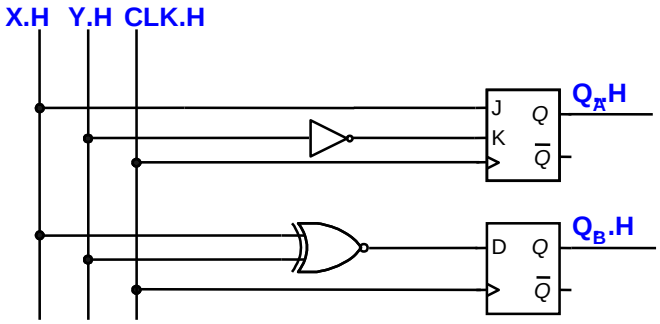
NOTE THAT THERE ARE OTHER POSSIBLE SOLUTIONS TOO…

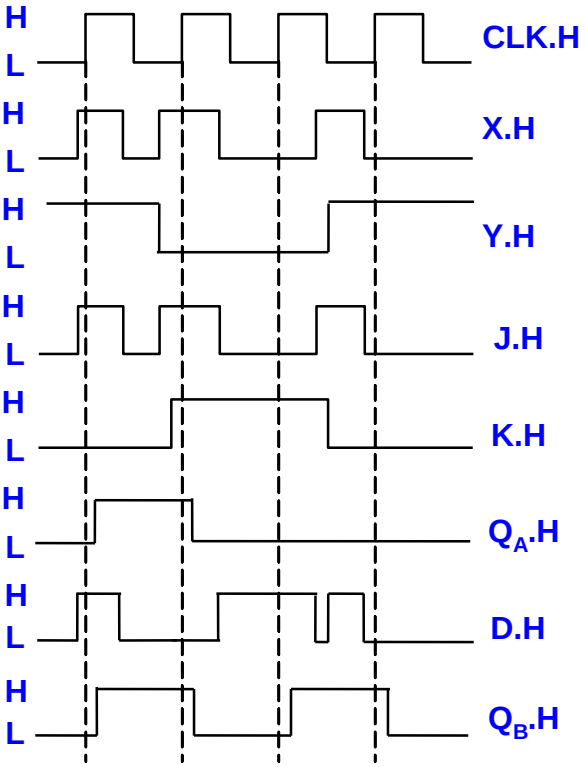
Question 1



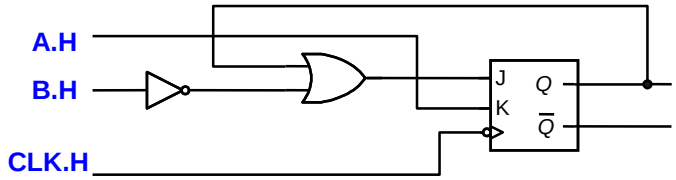
Assumption: The D input satisfies the set-up and hold times of the Latch and flip-flop. Also, the propagation delay of the devices are much less than the CLK period.

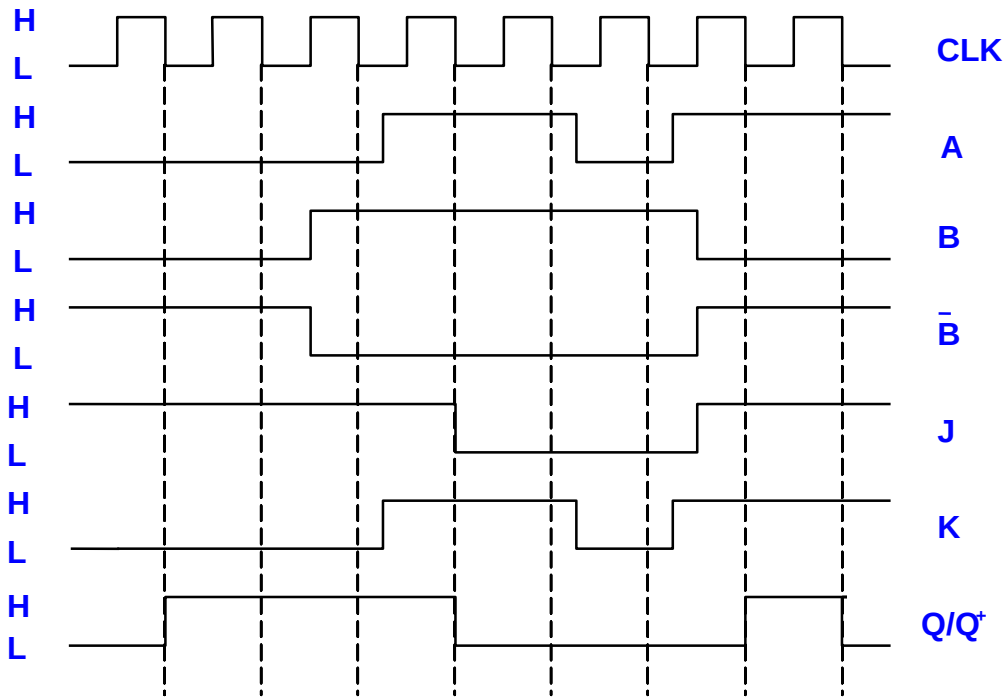
Question 2





Question 3





A	B	Q	Q^+
0	0	0	**1**
0	0	1	**1**
0	1	0	**0**
0	1	1	**1**
1	0	0	**1**
1	0	1	**0**
1	1	0	**0**
1	1	1	**0**

Characteristic Table

A	B	Q^+
0	0	**1**
0	1	**Q**
1	0	$\overline{Q}$
1	1	**0**

Condensed Characteristic Table